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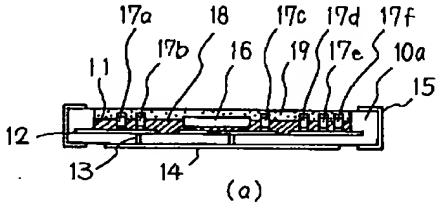
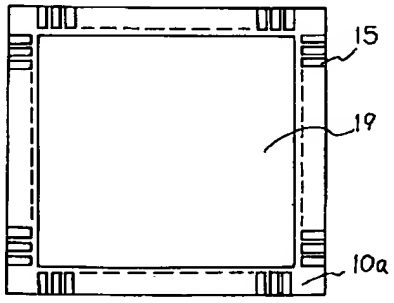
(54)【発明の名称】　混成集積回路装置およびその製造方法

(57)【要約】
【目的】対ノイズ性に優れた混成集積回路装置を提供する。
【構成】配線基板に凹部１１を設け、この凹部に半導体チップ１６もしくは受動チップ部品１７ａ～１７ｆまたはその両方を搭載して樹脂封止した構造を有し、凹部底面に対して半導体チップ１６はフェイスダウンで搭載し、受動チップ部品１７ａ～１７ｆは直立させて搭載することによって半導体チップ１６の裏面および受動チップ部品の一方側電極を凹部上方の向きにそろえ、半導体チップの裏面および受動チップ部品１７ａ～１７ｆの一方側電極が露出する高さまで非導電性封止樹脂１８を充填し、その上に導電性封止樹脂１９を充填して露出した裏面および一方側電極を覆うことによって、搭載部品の裏面もしくは一方側電極を導電性封止樹脂層１９に直接接触させて電気的接続をする。この導電性封止樹脂１９を電源電位または接地電位に接続してシールド構造を形成する。



(a)



(b)

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【特許請求の範囲】

【請求項１】　複数の内部導体層を有する多層の配線基板の一方面に所定の大きさおよび深さで凹部が開口され、この凹部の底面および他方面の前記内部導体層に形成された配線パターンに半導体チップまたは受動チップ部品のいずれかが少なくとも１つ接続されて搭載され、前記半導体チップ搭載時はその各電極が前記底面の配線パターンにワイヤボンディング接続され、前記受動チップ部品搭載時はその各電極が前記底面の配線パターンに導電性接着剤を用いて接続され、これら配線パターンはスルーホールを介して前記他方面の配線パターンにそれぞれ接続され、かつこれら配線パターンが前記凹部の周縁部側面に配設された端面電極にそれぞれ接続されるとともに、前記凹部内が樹脂封止されてなる混成集積回路装置において；前記樹脂封止は、前記底面側に充填される非導電性封止樹脂とこの非導電性封止樹脂上に充填される導電性封止樹脂とを含む多層構造からなり、前記導電性封止樹脂は、低位側電源電位または高位側電源電位のいずれかの電位が供給されかつ前記半導体チップの裏面側および前記受動チップ部品の他方電極側の少くとも一方側に直接接触させた構造を有することを特徴とする混成集積回路装置。

【請求項２】　前記半導体チップおよび前記受動チップ部品をそれぞれ少なくとも１つずつ搭載した請求項１記載の混成集積回路装置。

【請求項３】　前記凹部に少なくとも１つの半導体チップが搭載され、これら半導体チップはそれぞれフェイスダウンで各電極が前記底面の対応する配線パターンにバンプ接続され、前記非導電性封止樹脂は前記半導体チップの裏面が露出する高さまで充填され、これら露出した裏面を含む前記非導電性封止樹脂層上に前記導電性封止樹脂が積層されて封止される請求項１または２記載の混成集積回路装置。

【請求項４】　前記凹部に少なくとも１つの前記受動チップ部品が搭載され、これら受動チップ部品の少なくとも一部は、前記一方電極側のみ前記底面の配線パターンに接続されるように直立して搭載され、前記非導電性封止樹脂は前記受動チップ部品の前記他方電極側がそれぞれ露出する高さまで充填され、これら露出した前記他方電極側を含む前記非導電性封止樹脂層上に前記導電性封止樹脂が積層されて封止される請求項１または２記載の混成集積回路装置。

【請求項５】　前記開口により残された基板周縁部内にある前記内部導体層の全面に形成されたベタパターンが前記基板側面および底面周縁部を囲んで配設され導電体層と一体となり、かつ前記凹部内側壁面で前記導電性封止樹脂端面と電気的に接続させて形成したシールド層を有する請求項１、３または４記載の混成集積回路装置。

【請求項６】　複数の内部導体層を有する多層の配線基板の一方面に所定の大きさおよび深さで凹部を開口し、

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この凹部の底面および他方面の前記内部導体層に形成された配線パターンに半導体チップおよび受動チップ部品を少なくとも１つずつ接続して搭載し、前記半導体チップはその各電極を前記底面の配線パターンにワイヤボンディング接続し、前記受動チップ部品はその各電極を前記底面の配線パターンに導電性接着剤を用いて接着し、これら配線パターンをスルーホールを介して前記他方面の配線パターンにそれぞれ接続するとともに、前記凹部を樹脂封止する混成集積回路装置の製造方法において；前記配線基板の前記凹部に少なくとも１つの前記半導体チップをフェイスダウンで前記底面の配線パターンにバンプ接続する第１の工程と、前記工程終了後の前記配線基板に少なくとも１つの前記受動チップ部品を直立させた状態で一方側の電極のみを導電性接着剤により前記底面の配線パターンに接着およびキュアし硬化させる第２の工程と、前記バンプ接続された前記半導体チップの裏面および前記接着された前記受動チップ部品の他方側の電極がそれぞれ露出する高さまで前記凹部に非導電性封止樹脂を充填してキュアし硬化させる第３の工程と、前記硬化後の前記非導電性封止樹脂の上部に露出する前記裏面および前記電極のそれぞれを全て覆う高さまで導電性封止樹脂を充填してキュアし硬化させる第４の工程とからなる混成集積回路装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は混成集積回路装置に係わり、特に薄型でリードレスタイプの表面実装用混成集積回路装置のノイズ対策を施した混成集積回路装置に関する。

【０００２】

【従来の技術】近年、半導体素子の微細化が進み、半導体装置に収容される回路規模もさらに増大し、民生用機器、工業用機器、その他いろいろな産業分野からのニーズに応えるために多機能化とともに各種の実装形態の半導体装置が開発されてきた。

【０００３】これら実装形態の一つに混成集積回路装置がある。この装置は、配線基板上に形成された配線パターンで相互接続されるマイコン、メモリ、ゲートアレイ等のベアチップ、あるいは抵抗、コンデンサ等の受動チップ部品を混在して搭載し、システム規模の機能を実現しようとするものである。用途によっては、ベアチップのみ、あるいは受動チップ部品のみが搭載される場合ものもある。

【０００４】このように機能強化された混成集積回路装置に対する要求としては、高速化、高周波化、大電力化とともに、外来ノイズあるいは搭載チップ間で相互に影響を与えるノイズに対する対策がある。ノイズ対策を考慮したこの種の従来の混成集積回路装置の一例を断面図で示した図５を参照すると、配線基板３０の凹部３１の底面に、半導体チップ３２およびノイズフィルター用の

ものを含む受動チップ部品３３ａ～３３ｃを搭載する。その際、半導体チップ３２の電極と配線基板３０に配設された導体層による配線パターン３４は、ボンディングワイヤ３５によって電気的接続が行なわれ、受動チップ部品３３ａ～３３ｃは導電性接着剤等によって電気的接続が図られる。なお、半導体チップが素子形成面を下側に向けて（フェイスダウン）搭載するフリップチップの場合は配線基板面の電極との接続はハンダバンプにより行なわれる。

【０００５】また、配線基板３０の凹部３１は非導電性封止樹脂３６（図中の斜線部分）で封止し、必要に応じて、配線パターン３７を裏面に設けてスルーホール３８で配線パターン３４と貫通接続したり、封止表面にシールド板３９を接着することにより、シールド構造としていた。

【０００６】さらに、シールド板３９を設ける代りにパッケージ自体をマザーボードに対し裏返しに実装し、樹脂封止面と対応するマザーボードの表面に配線パターンを設ける場合もある。

【０００７】一方、受動チップ部品を搭載する方法の一例が、特開平３－２５６３９２号公報に記載されている。同公報記載の混成集積回路装置の断面図を示した図６を参照すると、受動チップ部品を直立させて搭載する場合の一例であり、この場合は、搭載電極４０ａに下側の電極４１ａを接続した受動チップ部品４２の上側の電極４１ｂと配線基板４３側の搭載電極４０ｂとをボンディングワイヤ４４を用いて接続している。

【０００８】前述したように、ノイズのアンテナとなりやすいボンディングワイヤを使用しなければならない点および、電極２４，２５が依然として基板面上に２つある点で他の従来例と同様である。

【０００９】

【発明が解決しようとする課題】この従来の混成集積回路装置では、受動チップ部品を搭載する場合に、その受動チップ部品が有する２つの電極が共に基板表面の配線パターンと直接またはワイヤにより接続されるため、接続用電極を２つそれぞれ基板上に確保しなければならず、実装面積が大きくなる。そのため、半導体チップ近傍の配線パターンの密集した部分には、受動チップ部品の配置（レイアウト）が難しいという問題があった。ノイズ除去のためには、発生源となる能動素子の出来るだけ近傍にバイパスコンデンサおよびフィルター回路を配置するのが効果的であるのにもかかわらず、上述したようにそれぞれ２つの接続用電極を基板上に設けなければならないという問題が、それを難しくしていた。

【００１０】一方、前述したバンプ接続により半導体チップを裏返しに搭載するフェイスダウンの手法はフリップチップ等でしばしば行われるが、裏面を電源電位または接地電位である安定電位に接続する方法としては確立されたものが無く、限られた半導体チップにしか適用出来ないという問題もあった。ノイズ防止のためには、ワイヤーがノイズのアンテナとなってしまうので、ワイヤーを用いることなく、かつ半導体チップ自体がシールド板の効果を持ち得る点でフェイスダウンで搭載する方が有利であるのは明らかであるが、上述したようにチップ裏面を安定電位に接続する方法が未確立のためその適用の範囲がせばめられていた。

【００１１】本発明の目的は、上述した問題点に鑑みなされたものであり、半導体チップをフェイスダウンで配線基板にバンプ接続して搭載し、かつその周辺回路部品の受動チップ部品とともにシールドを施した構造を有する混成集積回路装置およびその製造方法を提供することにある。

【００１２】

【課題を解決するための手段】本発明の混成集積回路装置の特徴は、複数の内部導体層を有する多層の配線基板の一方面に所定の大きさおよび深さで凹部が開口され、この凹部の底面および他方面の前記内部導体層に形成された配線パターンに半導体チップまたは受動チップ部品のいずれかが少なくとも１つ接続されて搭載され、前記半導体チップ搭載時はその各電極が前記底面の配線パターンにワイヤボンディング接続され、前記受動チップ部品搭載時はその各電極が前記底面の配線パターンに導電性接着剤を用いて接続され、これら配線パターンはスルーホールを介して前記他方面の配線パターンにそれぞれ接続され、かつこれら配線パターンが前記凹部の周縁部側面に配設された端面電極にそれぞれ接続されるとともに、前記凹部内が樹脂封止されてなる混成集積回路装置において；前記樹脂封止は、前記底面側に充填される非導電性封止樹脂とこの非導電性封止樹脂上に充填される導電性封止樹脂とを含む多層構造からなり、前記導電性封止樹脂は、低位側電源電位または高位側電源電位のいずれかの電位が供給されかつ前記半導体チップの裏面側および前記受動チップ部品の他方電極側の少くとも一方側に直接接触させた構造を有することにある。

【００１３】また、前記半導体チップおよび前記受動チップ部品をそれぞれ少なくとも１つずつ搭載することができる。

【００１４】さらに、前記凹部に少なくとも１つの半導体チップが搭載され、これら半導体チップはそれぞれフェイスダウンで各電極が前記底面の対応する配線パターンにバンプ接続され、前記非導電性封止樹脂は前記半導体チップの裏面が露出する高さまで充填され、これら露出した裏面を含む前記非導電性封止樹脂層上に前記導電性封止樹脂が積層されて封止されてもよい。

【００１５】さらにまた、前記凹部に少なくとも１つの前記受動チップ部品が搭載され、これら受動チップ部品の少なくとも一部は、前記一方電極側のみ前記底面の配線パターンに接続されるように直立して搭載され、前記非導電性封止樹脂は前記受動チップ部品の前記他方電極

側がそれぞれ露出する高さまで充填され、これら露出した前記他方電極側を含む前記非導電性封止樹脂層上に前記導電性封止樹脂が積層されて封止することができる。

【００１６】さらに、前記開口により残された基板周縁部内にある前記内部導体層の全面に形成されたベタパターンが前記基板側面および底面周縁部を囲んで配設され導電体層と一体となり、かつ前記凹部内側壁面で前記導電性封止樹脂端面と電気的に接続させて形成したシールド層を有することもできる。

【００１７】本発明の混成集積回路装置の製造方法の特徴は、複数の内部導体層を有する多層の配線基板の一方面に所定の大きさおよび深さで凹部を開口し、この凹部の底面および他方面の前記内部導体層に形成された配線パターンに半導体チップおよび受動チップ部品を少なくとも１つずつ接続して搭載し、前記半導体チップはその各電極を前記底面の配線パターンにワイヤボンディング接続し、前記受動チップ部品はその各電極を前記底面の配線パターンに導電性接着剤を用いて接着し、これら配線パターンをスルーホールを介して前記他方面の配線パターンにそれぞれ接続するとともに、前記凹部を樹脂封止する混成集積回路装置の製造方法において；前記配線基板の前記凹部に少なくとも１つの前記半導体チップをフェイスダウンで前記底面の配線パターンにバンプ接続する第１の工程と、前記工程終了後の前記配線基板に少なくとも１つの前記受動チップ部品を直立させた状態で一方側の電極のみを導電性接着剤により前記底面の配線パターンに接着およびキュアし硬化させる第２の工程と、前記バンプ接続された前記半導体チップの裏面および前記接着された前記受動チップ部品の他方側の電極がそれぞれ露出する高さまで前記凹部に非導電性封止樹脂を充填してキュアし硬化させる第３の工程と、前記硬化後の前記非導電性封止樹脂の上部に露出する前記裏面および前記電極のそれぞれを全て覆う高さまで導電性封止樹脂を充填してキュアし硬化させる第４の工程とからなることにある。

【００１８】

【作用】本発明の混成集積回路は、配線パターン形成用の内部導体配線層を有する多層の配線基板の、基板周縁部を除く上面部分に凹部を形成して導体配線層の一部を露出させる。まず、この凹部にバイパスコンデンサ、フィルター等を形成するための受動チップ部品もしくはチップジャンパー等を搭載する場合には、これらのチップ部品の片側の電極のみを配線基板に電気的に接続するように直立させてマウントしておき、凹部底面からチップ部品の下側の電極を含み上側の電極が露出する高さまで非導電性封止樹脂を充填・キュアして硬化させる。さらに非導電性封止樹脂の上にチップ部品の上側の電極を覆う高さまで導電性封止樹脂を充填・キュアして積層することにより、上側電極を導電性封止樹脂層に直接接触させることで電気的接続がとれるようにした。

【００１９】また、凹部に半導体チップを搭載する場合には、半導体チップの素子形成面を下向きにしたいわゆるフェイスダウンで搭載しておき、この凹部底面から半導体チップ裏面部分が露出する高さまで非導電性封止樹脂を充填・キュアして硬化させ、さらに非導電性封止樹脂の上に半導体チップの露出した裏面部分を覆う高さまで導電性封止樹脂を充填・キュアすることにより裏面部分を導電性封止樹脂層に直接接触させる形で電気的接続がとれるようにしてある。

【００２０】また、上述したいずれの場合も、導電性封止樹脂層自体を外部から供給される安定電位へ接続する場合は、チップジャンパーを介して配線基板内の安定電位に対応する配線パターンと接続するか、予め配線基板の凹部に充填される導電性封止樹脂に電気的接続がとれるように、周縁部上面に近い内部導体層を全面ベタパターンとして形成し、かつ基板側面および底面周縁部を囲んで配設した導電体層と一体となってシールド層を形成し、外部電極を介してこのシールド層に供給される安定電位が導電性封止樹脂を介して半導体チップの裏面にも供給されるようにしてある。

【００２１】したがって、導電性封止樹脂がシールドの役目を果すことが出来ることになる。

【００２２】

【実施例】次に、本発明について図面を参照しながら説明する。

【００２３】図１（ａ）は本発明の第１の実施例の断面図であり、図１（ｂ）その平面図である。図１（ａ）および図１（ｂ）を参照すると、例えばガラスエポキシ樹脂からなる多層配線基板１０ａの上面の、周縁部以外の部分に凹部１１を開口する。この開口部の大きさおよび深さは、搭載される部品の大きさおよび数量によって予め決められている。この開口により凹部１１の底面には搭載する構成部品間を接続するために予め配設された配線パターン１２が露出される。この配線パターン１２はスルーホール１３により必要に応じて裏面側に配設された配線パターン１４に適宜接続されている。

【００２４】さらに、裏面側の配線パターン１４は、直接あるいは搭載された構成部品を介して間接的に、基板周縁部に配設された端面電極１５に配線パターン１４を用いて所定の接続がなされている。この端面電極１５はいわゆるパッケージの外部端子であって、互いに間隔をおいて並べられた導体群からなり、複数の異る電位を有している。

【００２５】上述した配線基板１０の凹部１１に、例えば半導体チップ１６と、チップジャンパーを含む受動チップ部品１７ａ～１７ｆが搭載されている。この半導体チップ１６はフェイスダウンで各電極が配線パターン１２にそれぞれバンプ接続されている。

【００２６】一方、受動チップ部品１７ａ～１７ｆは、従来例の場合はチップ自身の有する２つの電極はそれぞ

れ凹部底面側の配線パターン１２に接続されていたが、本実施例においては、一方側の電極のみ配線パターン１２にそれぞれ接続された状態で直立して搭載される。

【００２７】凹部１１は底面から半導体チップ１６の裏面および受動チップ部品１７ａ～１７ｆの他方側の電極がそれざれ露出する高さまで非導電性封止樹脂１８（図中斜線状の網目で示す）が充填されている。この非導電性封止樹脂１８の上には基板周縁部上面と同じ高さまで導電性封止樹脂１９（図中点状の網目で示す）が充填されて樹脂封止が行なわれている。

【００２８】導電性封止樹脂１９は、例えばチップジャンパーを受動チップ部品１７ｂとすると、チップジャンパー１７ｂにより配線パターン１２、スルーホール１３および配線パターン１４のうちの所定のパターン（不図示）を介して端面電極１５のうちの電源電位または接地電位の安定電位が外部から供給される電極に電気的接続がなされている。

【００２９】本実施例に示した構造により、導電性封止樹脂１９が、半導体チップ１６の裏面および受動チップ部品１７ａ～１７ｂの他方側電極を安定電位に接続するので、シールド効果を得ることが出来る。

【００３０】本発明の第２の実施例を断面図で示した図２（ａ）およびその平面図を示した図２（ｂ）を参照すると、側面シールド構造を有するパッケージを構成した場合の例である。第の１実施例において、端面電極１５はいわゆるパッケージの外部端子であって、互いに間隔をおいて並べられた導体群を成し複数の異る電位を有していたが、第２の実施例では、これらは接地電位または電源電位等の安定電位を有する基板周辺部全面に渡って配設された単一のベタパターンとなっている。

【００３１】すなわち、第１の実施例との相違点は、導電性封止樹脂１９が配線基板１０ｂの内部導体層２０ａと凹部内側壁面で接触するとともに、内部導体層２０ａは配線基板１０ｂの側面２０ｂおよび底面周縁部２０ｃまで延長された側面シールド構造（断面図では２０ａ～２０ｂ～２０ｃで表わした略「コの字」型になる）であって配線基板１０ｂの周縁部全面を側面から囲むように配設され、かつその底面周縁部２０ｃには外部電極２１が設けられ、さらに、裏面側の配線パターン１４は、直接あるいは搭載された構成部品を介して間接的に、配線パターン１２はスルーホール１３を介して、それぞれ配線基板１０ｂの底面周縁部２０ｃの内側にあり、かつ外部電極領域２２に設けられた外部電極２３に接続されていることである。それ以外の構成要素は第１の実施例と同様であるからここでの構成の説明は省略する。

【００３２】上述した第２の実施例の構成によれば、延長された内部導体層２０ａ～２０ｃに外部電極２１から安定電位が供給されて、これらの延長された内部導体層２０ａ～２０ｃによりシールド効果を得ることが出来る。

【００３３】なお、上述した実施例の変形例として、導電封止樹脂層を複数層設け場合の断面図を示した図３（ａ）を参照すると、電樹脂封止層１８ｂの上に導電封止樹脂層１９ａと非導電樹脂封止層１８ａと導電封止樹脂層１９ａとが順次に積層されて形成されている。受動チップ部品１７ａと１７ｂの他方側の電極が導電封止樹脂層１９ａに接続され、半導体おチップ１６と受動チップ部品１７ｃおよび１７ｄとの裏面と他方側電極とが導電封止樹脂層１９ｂに接続されるので、搭載部品ごとに異なる安定電位のいずれかに分けて供給することができる。

【００３４】また、凹部を複数個設けた場合の断面図を示した図３（ｂ）を参照すると、凹部１１ａには受動チップ部品１７ａと半導体チップ１６が搭載され、凹部１１ｂには受動チップ部品１７ｂ～１７ｄが搭載されており、凹部毎にそれぞれ独立した機能をもたせることができる。

【００３５】上述した第１および第２の実施例で説明した混集積回路装置の製造方法は、その製造工程断面図であって、半導体チップのバンプ接続工程を示した図４（ａ）、受動チップ部品を接着する第２の工程示した図４（ｂ）、凹部に非導電性封止樹脂を充填する第３の工程を示した図４（ｃ）および導電性封止樹脂を充填する第４の工程を示した図４（ｄ）を参照すると、まず、ガラスエポキシ樹脂基板に公知のエッチング処理により形成した多層配線基板１０ａまたは１０ｂに凹部が形成された配線基板であって、この凹部に少なくとも１つの半導体チップ１６を公知の半田バンプ等の方法によりフェイスダウンで搭載する（図４（ａ））。

【００３６】次に、ノイズフィルタ用のものを含む受動チップ部品１７ａ～１７ｆを直立させた状態で、それぞれの片側（下側）の電極のみを導電性接着剤等によりマウントした後、キュアし、硬化させる（図４（ｂ））。

【００３７】しかる後、エポキシ系の絶縁性の高い非導電性封止樹脂１８を用いて所定の深さまで充填する。このとき、少なくとも、半導体チップ１６および受動チップ部品１７ａ～１７ｆのそれぞれの下側電極に接する配線パターン１２と電気的に接続する部分を全て覆いかくし、かつ、半導体チップ１６の裏面部分と、受動チップ部品１７ａ～１７ｆの上側電極は全て露出する高さまで充填して１５０°３０分前後でキュアし硬化させる（図４（ｃ））。

【００３８】さらに、しかる後、非導電性封止樹脂１８の上面および、この非導電性封止樹脂から露出する受動チップ部品１７ａ～１７ｆの全ての電極と半導体チップ１６の裏面とを覆う高さまで、Ｃｕペースト等の電導率の高い導電性封止樹脂１９を充填して、１５０°３０分前後でキュアし硬化させる（図４（ｄ））。

【００３９】なお、第４の工程の後、図には示さないが必要に応じてレジスト等の保護層をその上部に印刷形成

しても良い。

【００４０】第２の実施例の製造方法の場合、第１の工程における配線基板１０ｂは、基板周辺部全面に渡って配設される単一のベタパターンとして、側面シールド構造２０ｂ，２０ｃと一体となるよに内部導体層２０ａを予め設けておく。この導体層の高さ方向の位置は、導電性封止樹脂１９で封止する際に内部導体層２０ａの凹部内側壁面に露出した部分が導電性封止樹脂１９の端面に接触するように、導電性封止樹脂１９の層の厚みの範囲を勘案して決められる。

【００４１】さらに、配線基板１０ｂの裏面側は、外部端子としての突起電極２３が側面シールド構造２０ｃより内側の、基板周縁部２２に配設され、かつ凹部底面の配線パターン１２にそれぞれ接続されたものが使用される以外は、上述の製造工程と同様である。

【００４２】なお、非導電性封止樹脂１８の高さ、即ち層厚については、現状の半導体チップ１６の厚さが０．３ｍｍ～０．４ｍｍ程度、バンプ高さが０．１ｍｍ程度、受動チップ部品１７ａ～１７ｆの電極厚が０．２ｍｍ前後であることを想定すると、約０．２５ｍｍ～０．３５ｍｍ程度の間に調整すればよいことになる。

【００４３】０．１ｍｍ程度の巾の高さ調整は、現状の技術で何ら問題はない。勿論、半導体チップ１６、または受動チップ部品１７ａ～１７ｆのいずれか一方にのみ適用する場合は、その一方のみを考慮すればよいから上述した巾の余裕度はさらに広がることになる。

【００４４】以上説明したように、本発明の混成集積回路装置およびその製造方法によれば、例えば、前述したように、電源電位および接地電位間のバイパスコンデンサおよび各ノイズフィルタは、ノイズ発生源である半導体チップに可能な限り近い位置に配置しなければならないが、本発明の混成集積回路装置では、その構成要素の受動チップ部品を直立させて搭載出来ると同時に、片側の電極は凹部内のいたる所で安定電位に接続出来るため、配線基板のパターンレイアウトが極めて容易となる。さらに、直立させることによって搭載面積が本来の１／２以下となるので、パターン配設密度の高い半導体チップ近傍にも容易に配置出来、従って、より効果的なノイズ除去が可能になる。

【００４５】また、半導体チップの搭載においては、裏面部分を安定電位へ容易に接続する手段を提供出来るので、フリップチップ搭載の適用範囲が格段に広げられる。前述したように、ボンディングワイヤによる接続は、ワイヤーがアンテナとなり易く、しかも、搭載面積が約２倍を要して、その分バイパスコンデンサおよびフィルター用受動チップ部品も半導体チップから遠ざかることになるので、ノイズ的にもフリップチップでの搭載が明らかに有利である。

【００４６】また、半導体チップと受動チップ部品混在の場合は、特にそれぞれに必要な安定電位への接続を、プロセスを分けることなく一括の処理で行える点が非常に有効な効果である。

【００４７】多くの場合、搭載部品の高さの不一致から、基板導体層や印刷導体層もしくはシールド金属板の接着等では安定な接続を望めないが、本発明の混成集積回路装置のように、導電性封止樹脂の充填によれば、搭載部品の高さのバラツキをことごとく吸収し、安定な接続を得ることが可能になる。

【００４８】さらに、第２の実施例に示したように、導電性封止樹脂と基板内部導体層との電気的接続をとることも容易で、これを用いれば、導電性封止樹脂自体の外部回路の安定電位への接続が出来、従ってそれらが一体となったパッケージ上方向に対する良好なノイズシールド構造をも同時に実現出来る。

【００４９】さらにまた、第２の実施例のようにパッケージの側面をもメッキ処理等によりシールドし、裏面ベタパターンにまで接続し、側面導体下部とこの混成集積回路装置を搭載するマザーボード間の半田シール等も併用すれば２０ｄＢ～３０ｄＢのノイズ低減も出来る。

【００５０】また、副次的効果として本発明の構造によれば、半導体チップ裏面が、直接に熱伝導率の大きい導電性封止樹脂に接しており、その層厚も数百μと比較的厚くなるので、良好な放熱構造としても機能する。特に、前述したシールド構造をとった場合は、シールドの導体部分を介して配線基板側への熱放散が図られるのでより効果的である。

【００５１】熱によるＩＣデバイスの諸特性のシフトは、通常誤動作に対するノイズマージンを悪化させる。よって放熱構造は、ノイズ的観点から見ても重要な要素である。

【００５２】

【発明の効果】以上説明したように本発明の混成集積回路装置およびその製造方法は、配線基板に凹部を設け、この凹部に半導体チップもしくは受動チップ部品またはその両方を搭載し樹脂封止する構造であって、凹部底面に対して半導体チップはフェイスダウンで搭載し、受動チップ部品は直立させて搭載することによって半導体チップの裏面および受動チップ部品の一方側の電極を凹部上方の向きにそろえることにより、底面に接続した他方側の電極に対して垂直方向に離した状態を形成するとともに、凹部封止用樹脂が凹部底面に接する非導電性封止樹脂層とその上層の導電性封止樹脂層とを含む多層構造を有し、凹部底面から半導体チップ裏面部分および受動部チップ部品の一方側の電極が露出する高さまで非導電性封止樹脂を充填・キュアして硬化させ、さらに露出した裏面部分および一方側の電極を覆う高さまで非導電性封止樹脂の上に導電性封止樹脂を充填・キュアすることにより、裏面部分および一方側の電極をそれぞれ導電性封止樹脂層に直接接触させた状態で電気的接続がとれるようにしたので、導電性封止樹脂層を外部端子を介して

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安定電位に接続することにより、導電性封止樹脂層がノイズに対して極めて有効なシールド効果を果すことが出来る。

【００５３】また、導電性樹脂層と端面接触するようにした基板周縁部の内部導体層を基板側面および底面周縁部を囲んで形成した導電体層と一体となるようにしたシールド構造とすることも出来るので、同様なシールド効果が得られる。

【００５４】さらに、フリップチップ搭載適用の容易化，受動チップ部品によるフィルタ素子の自由度の高いレイアウト，良好なシールド構造および放熱構造のいずれも同時に実現出来るので、ノイズ対策が極めて容易かつ効果的に行え、デバイス本来の性能を充分に引き出すことを可能にしている。

【図面の簡単な説明】

【図１】（ａ）本発明の第１の実施例の混成集積回路装置を示す断面図である。

（ｂ）第１の実施例の平面図である。

【図２】（ａ）本発明の第２の実施例の混成集積回路装置を示す断面図である。

（ｂ）第２の実施例の平面図である。

【図３】（ａ）導電封止樹脂層を複数層設け場合の断面図である。

（ｂ）凹部を複数個設けた場合の断面図である。

【図４】（ａ）半導体チップのバンプ接続工程を示した断面図である。

（ｂ）受動チップ部品を接着する第２の工程示した断面図である。

（ｃ）凹部に非導電性封止樹脂を充填する第３の工程を示した断面図である。

12

＊（ｄ）導電性封止樹脂を充填する第４の工程を示した断面図である。

【図５】従来の混成集積回路装置の一例を示す断面図である。

【図６】従来の混成集積回路装置の他の例を示す断面図である。

【符号の説明】

１０ａ，３０，４３　　配線基板

１０ｂ　　側面シールド構造を有する配線基板

１１，１１ａ，１１ｂ　　３１　　凹部

１２，３４　　底面側の配線パターン

１３，３８　　スルーホール

１４，３７　　裏面側の配線パターン

１５　　端面電極

１６，３２　　半導体チップ

１７ａ～１７ｆ，３３ａ～３３ｃ，４２　　受動チップ部品

１８，１８ａ，１８ｂ，３６　　非導電封止樹脂

１９，１９ａ，１９ｂ　　導電性封止樹脂

２０ａ　　内部導体層（導体ベタパターン）

２０ｂ　　配線基板１０の側面シールド

２０ｃ　　底面周縁部シールド

２１，２２　　突起電極（外部電極）

２３　　外部電極領域

３５，４４　　ワイヤ

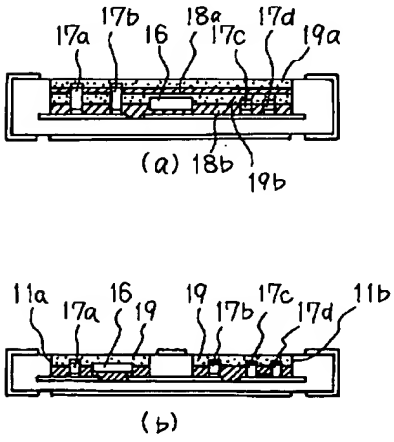
３９　　シールド板

４０ａ，４０ｂ　　搭載電極

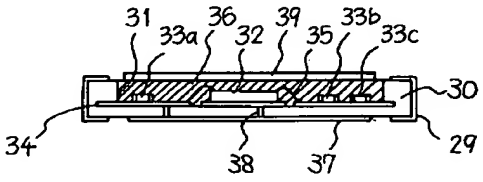
４１ａ　　受動チップ部品の上側電極

４１ｂ　　受動チップ部品の下側電極

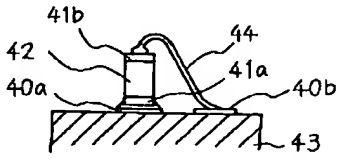
【図３】



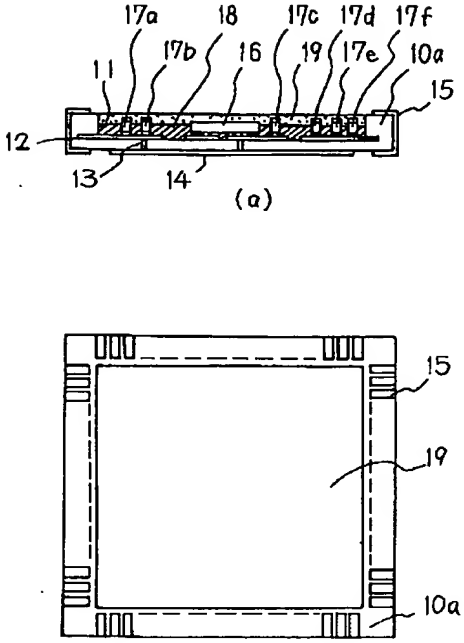
【図５】



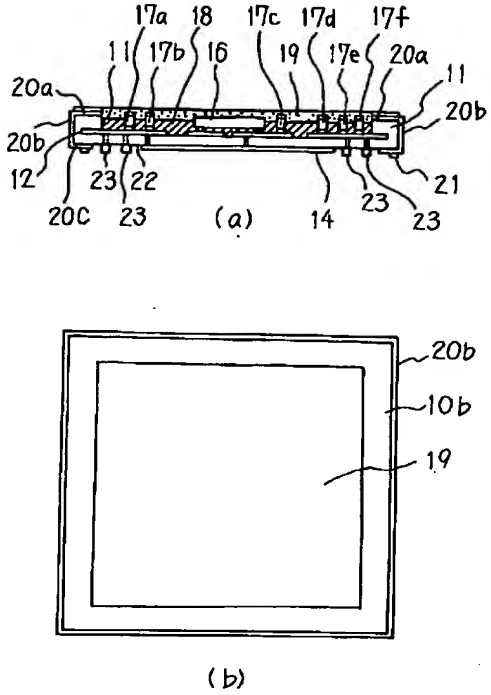
【図６】



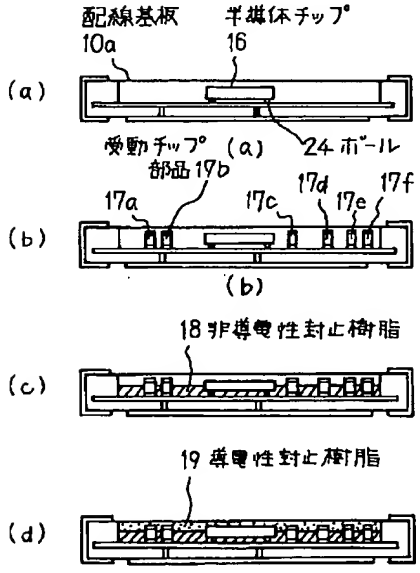
【図１】


17a
18
17c
17d
17f
17b
16
19
17e
10a
11
15
12
13
14
(a)
15
19
10a
(b)

【図２】


17a
18
17c
17d
17f
11
17b
16
19
17e
20a
20a
11
20b
20b
12
23
22
21
20C
23
(a)
14
23
23
20b
10b
19
(b)

【図４】


配線基板
半導体チップ
10a
16
(a)
受動チップ部品
(a)
24 ボール
17b
17a
17c
17d
17e
17f
(b)
(b)
18 非導電性封止樹脂
(c)
19 導電性封止樹脂
(d)

PATENT ABSTRACTS OF JAPAN

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H01L 25/18
H05K 3/28

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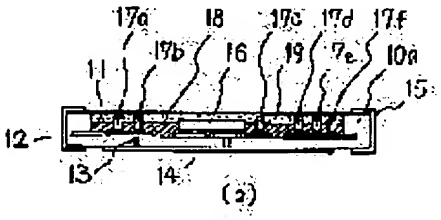
(22)Date of filing : 28.02.1995

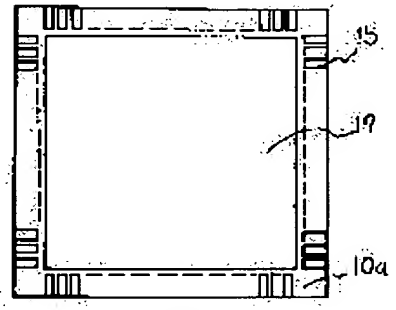
(71)Applicant : NEC CORP
(72)Inventor : EGAWA HIDENORI

(54) HYBRID INTEGRATED CIRCUIT DEVICE AND MANUFACTUR THEREOF

(57)Abstract:
PURPOSE: To realize quite effective noise shield effect by feeding a low or high power supply potential to a conductive sealing resin directly touching at least one of the rear side of a semiconductor chip or the other electrode side of a passive chip device.
CONSTITUTION: Wiring patterns 12, 14 are connected, respectively, with end face electrodes 15 arranged on the circumferential side face of a resin sealed recess 11. In this regard, a multilayer resin sealing structure comprising a nonconductive sealing resin 18 filling the bottom face side and a conductive sealing resin 19 filling the upper part thereof is employed. The conductive sealing resin 19 is applied with any one of low or high power supply potentials and constructed to touch at,least one of the rear side of a semiconductor chip 16 or the other electrode side of passive chip device 17a-17f directly. With such structure, quite effective noise shield effect is provided by the conductive sealing resin 19.



(a)



(b)

LEGAL STATUS

[Date of request for examination]	28.02.1995
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	2630294
[Date of registration]	18.04.1997
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	18.04.2005

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] Opening of the crevice is carried out in the multilayer magnitude of a wiring substrate predetermined on the other hand to a field and the multilayer depth which have two or more inner conductor layers. Either [at least one] a semiconductor chip or a passive chip is connected to the circuit pattern formed in said inner conductor layer of the base of this crevice, and an another side side, and it is carried. Wirebonding connection of each of that electrode is made at the circuit pattern of said base at the time of said semiconductor chip loading. At the time of said passive chip element placement, each of that electrode uses electroconductive glue for the circuit pattern of said base, and is connected to it. While connecting with the end-face electrode with which these circuit patterns were connected to the circuit pattern of said another side side through the through hole, respectively, and these circuit patterns were arranged in the periphery section side face of said crevice, respectively In the hybrid integrated circuit equipment with which it comes to carry out the resin seal of the inside of said crevice the; aforementioned resin seal It consists of multilayer structure containing the non-conductive closure resin with which said base side is filled up, and the conductive closure resin with which it fills up on this non-conductive closure resin. Said conductive closure resin Hybrid integrated circuit equipment characterized by supplying the potential of either lower order side power-source potential or high order side power-source potential, and having the structure by the side of the rear face of said semiconductor chip, and the another side electrode of said passive chip where one side was made to contact directly at least.
[Claim 2] Hybrid integrated circuit equipment according to claim 1 which carried every at least one of said semiconductor chip and said the passive chips, respectively.
[Claim 3] It is hybrid integrated circuit equipment according to claim 1 or 2 with which it fills up with said non-conductive closure resin to the height which the rear face of said semiconductor chip exposes, and the laminating of said conductive closure resin is carried out, and the closure is carried out on said non-conductive closure resin layer including the these-exposed rear face by carrying at least one semiconductor chip in said crevice, and making bump connection of each electrode by face down at the circuit pattern with which said base corresponds, respectively, as for these semiconductor chips.
[Claim 4] Said at least one passive chip is carried in said crevice. Some these passivity chips [at least] It is stood straight and carried so that only the aforementioned one side electrode side may be connected to the circuit pattern of said base. Said non-conductive closure resin is hybrid integrated circuit equipment according to claim 1 or 2 with which the laminating of said conductive closure resin is carried out, and the closure is carried out on said non-conductive closure resin layer with which it fills up, and which contains said these-exposed another side electrode side to the height which said another side electrode side of said passive chip exposes, respectively.
[Claim 5] Hybrid integrated circuit equipment according to claim 1, 3, or 4 which has the shielding layer in which it was surrounded and arranged, and it is united with a conductor layer, and the solid pattern formed all over said inner conductor layer in the substrate periphery circles left behind by said opening made it connect with said conductive closure resin end face electrically on said crevice inside wall surface, and formed said substrate side face and the base periphery section.
[Claim 6] Opening of the crevice is carried out in the multilayer magnitude of a wiring substrate predetermined on the other hand to a field and the multilayer depth which have two or more inner conductor layers. A semiconductor chip and every at least one passive chip are connected and carried in the circuit pattern formed in said inner conductor layer of the base of this crevice, and an another side side. Said semiconductor chip makes wirebonding connection of each of that electrode at the circuit pattern of said base. While said passive chip uses electroconductive glue at the circuit pattern of said base, pastes up each of that electrode and connects these circuit patterns to the circuit pattern of said another side side through a through hole, respectively The 1st process which makes bump connection of said at least one semiconductor chip by face

down in said crevice of the; aforementioned wiring substrate at the circuit pattern of said base in the manufacture approach of the hybrid integrated circuit equipment which carries out the resin seal of said crevice, The 2nd process which a cure is pasted up and carried out [process] and makes said wiring substrate after said process termination harden only the electrode of one side to the circuit pattern of said base with electroconductive glue where said at least one passive chip is uprighted, The 3rd process at which the rear face of said said semiconductor chip by which bump connection was made, and the electrode of the other side of said said pasted-up passive chip fill up with and carry out the cure of the non-conductive closure resin to said crevice, and make it harden it to the height exposed, respectively, The manufacture approach of the hybrid integrated circuit equipment which consists of the 4th process which it is filled [process] up with conductive closure resin, and the cure of each of said rear face exposed to the upper part of said non-conductive closure resin after said hardening and said electrode all is carried out [process], and stiffens it to wrap height.

[Translation done.]

* NOTICES *

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3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the hybrid integrated circuit equipment which took the measures against a noise of the lead loess type hybrid integrated circuit equipment for surface mounts with the thin shape with respect to hybrid integrated circuit equipment.
[0002]
[Description of the Prior Art] Detailed-ization of a semiconductor device progresses in recent years, and in order that the circuit scale held in a semiconductor device may also increase further and may respond to needs from consumer appliances, an industrial use device, and other various industrial fields, the semiconductor device of various kinds of mounting gestalten has been developed with multi-functionalization.
[0003] Hybrid integrated circuit equipment is in one of the mounting gestalten of these. This equipment tends to intermingle for them and carry passive chips, such as bare chips, such as a microcomputer which interconnects with the circuit pattern formed on the wiring substrate, memory, and a gate array, or resistance, and a capacitor, and tends to realize the function of a system scale. When only a bare chip or a passive chip is carried depending on an application, there is also a thing.
[0004] Thus, as a demand to the hybrid integrated circuit equipment by which functional enhancement was carried out, a cure in the noise which affects it mutually between an outpatient department noise or a loading chip is with improvement in the speed, high-frequency-izing, and large electrification. Reference of drawing 5 which showed an example in consideration of the cure against a noise of this kind of conventional hybrid integrated circuit equipment with the sectional view carries the passive chips 33a-33c containing the thing a semiconductor chip 32 and for noise filters in the base of the crevice 31 of the wiring substrate 30. In that case, electrical installation is performed by the bonding wire 35 and, as for the circuit pattern 34 by the conductor layer arranged by the electrode and the wiring substrate 30 of a semiconductor chip 32, electrical installation is planned by electroconductive glue etc., as for the passive chips 33a-33c. In addition, in the case of the flip chip to which a semiconductor chip turns a component forming face to the bottom, and carries it (face down), connection with the electrode of a wiring substrate side is made by the pewter bump.
[0005] Moreover, the crevice 31 of the wiring substrate 30 was made into shielding structure by closing by non-conductive closure resin 36 (shadow area in drawing), forming a circuit pattern 37 in a rear face if needed, carrying out interface connection to a circuit pattern 34, or pasting up the shielding plate 39 on a closure front face in a through hole 38.
[0006] Furthermore, the package itself may be mounted inside out to a mother board instead of forming the shielding plate 39, and a circuit pattern may be prepared in a resin seal side and the front face of a corresponding mother board.
[0007] On the other hand, an example of an approach which carries a passive chip is indicated by JP,3-256392,A. If drawing 6 R> 6 which showed the sectional view of hybrid integrated circuit equipment given in an official report is referred to, it will be an example in the case of uprighting a passive chip and carrying it, and loading electrode 40b by the side of this electrode 41b of the passive chip 42 top which connected lower electrode 41a to loading electrode 40a and wiring substrate 43 will be connected in this case using a bonding wire 44.
[0008] As mentioned above, it is the same as that of the conventional example of others [the point which must use the bonding wire which is easy to serve as an antenna of a noise, and the point which still has electrodes 24 and 25 on / two / a substrate side].
[0009]
[Problem(s) to be Solved by the Invention] With this conventional hybrid integrated circuit equipment, since both two electrodes that that passive chip has are connected by the circuit pattern on the front face of a substrate,

direct, or the wire when it carries a passive chip, two electrodes for connection must be secured on a substrate, respectively, and a component-side product becomes large. Therefore, there was a problem that arrangement (layout) of a passive chip was difficult in the part in which the circuit pattern near the semiconductor chip crowded. For noise rejection, although it was effective for near to have arranged [of the active element used as a generation source] a bypass capacitor and a filter circuit as much as possible, the problem that two electrodes for connection had to be prepared on a substrate, respectively as mentioned above made it difficult.
[0010] Although the technique of the face down which carries a semiconductor chip inside out by bump connection mentioned above on the other hand was often performed by the flip chip etc., there was also a problem that there was nothing that was established as an approach of connecting a rear face to the stabilization potential which is power-source potential or touch-down potential, and it could apply only to the limited semiconductor chip. for noise prevention , since the wire became the antenna of a noise , it be clear that it be more advantageous to carry by face down in that the semiconductor chip itself can have the effectiveness of a shielding plate , without use a wire , but since the approach of connect a chip rear face to stabilization potential had not be established as mention above , the range of the application be narrowed .
[0011] The purpose of this invention is to offer the hybrid integrated circuit equipment which has the structure which was made in view of the trouble mentioned above, made bump connection, and carried the semiconductor chip in the wiring substrate by the face down, and shielded with the passive chip of the circumference passive circuit elements, and its manufacture approach.
[0012]
[Means for Solving the Problem] Opening of the crevice is carried out in the multilayer magnitude of a wiring substrate predetermined on the other hand to a field and the multilayer depth in which the description of the hybrid integrated circuit equipment of this invention has two or more inner conductor layers. Either [at least one] a semiconductor chip or a passive chip is connected to the circuit pattern formed in said inner conductor layer of the base of this crevice, and an another side side, and it is carried. Wirebonding connection of each of that electrode is made at the circuit pattern of said base at the time of said semiconductor chip loading. At the time of said passive chip element placement, each of that electrode uses electroconductive glue for the circuit pattern of said base, and is connected to it. While connecting with the end-face electrode with which these circuit patterns were connected to the circuit pattern of said another side side through the through hole, respectively, and these circuit patterns were arranged in the periphery section side face of said crevice, respectively In the hybrid integrated circuit equipment with which it comes to carry out the resin seal of the inside of said crevice the; aforementioned resin seal It consists of multilayer structure containing the non-conductive closure resin with which said base side is filled up, and the conductive closure resin with which it fills up on this non-conductive closure resin. Said conductive closure resin It is in the potential of either lower order side power-source potential or high order side power-source potential being supplied, and having the structure by the side of the rear face of said semiconductor chip, and the another side electrode of said passive chip where one side was made to contact directly at least.
[0013] Moreover, every at least one of said semiconductor chip and said the passive chips can be carried, respectively.
[0014] Furthermore, at least one semiconductor chip is carried in said crevice, as for these semiconductor chips, bump connection of each electrode is made by face down at the circuit pattern with which said base corresponds, respectively, to the height which the rear face of said semiconductor chip exposes, on said non-conductive closure resin layer with which it fills up and which includes the these-exposed rear face, the laminating of said conductive closure resin may be carried out, and the closure of said non-conductive closure resin may be carried out.
[0015] Said at least one passive chip is carried in said crevice further again. Some these passivity chips [at least] It is stood straight and carried so that only the aforementioned one side electrode side may be connected to the circuit pattern of said base. To the height which said another side electrode side of said passive chip exposes, respectively, the laminating of said conductive closure resin is carried out on said non-conductive closure resin layer with which it fills up and which contains said these-exposed another side electrode side, and said non-conductive closure resin can be closed.
[0016] Furthermore, it can also have the shielding layer in which it was surrounded and arranged, and it is united with a conductor layer, and the solid pattern formed all over said inner conductor layer in the substrate periphery circles left behind by said opening made it connect with said conductive closure resin end face electrically on said crevice inside wall surface, and formed said substrate side face and the base periphery section.
[0017] The description of the manufacture approach of the hybrid integrated circuit equipment of this invention Opening of the crevice is carried out in the multilayer magnitude of a wiring substrate predetermined on the

other hand to a field and the multilayer depth which have two or more inner conductor layers. A semiconductor chip and every at least one passive chip are connected and carried in the circuit pattern formed in said inner conductor layer of the base of this crevice, and an another side side. Said semiconductor chip makes wirebonding connection of each of that electrode at the circuit pattern of said base. While said passive chip uses electroconductive glue at the circuit pattern of said base, pastes up each of that electrode and connects these circuit patterns to the circuit pattern of said another side side through a through hole, respectively The 1st process which makes bump connection of said at least one semiconductor chip by face down in said crevice of the; aforementioned wiring substrate at the circuit pattern of said base in the manufacture approach of the hybrid integrated circuit equipment which carries out the resin seal of said crevice, The 2nd process which a cure is pasted up and carried out [process] and makes said wiring substrate after said process termination harden only the electrode of one side to the circuit pattern of said base with electroconductive glue where said at least one passive chip is uprighted, The 3rd process at which the rear face of said said semiconductor chip by which bump connection was made, and the electrode of the other side of said said pasted-up passive chip fill up with and carry out the cure of the non-conductive closure resin to said crevice, and make it harden it to the height exposed, respectively, It is in consisting of the 4th process which it is filled [process] up with conductive closure resin, and the cure of each of said rear face exposed to the upper part of said non-conductive closure resin after said hardening and said electrode all is carried out [process], and stiffens it to wrap height.

[0018]

[Function] the top-face part except the substrate periphery section of the multilayer wiring substrate with which the hybrid integrated circuit of this invention has an inner conductor wiring layer for circuit pattern formation -- a crevice -- forming -- a conductor -- a part of wiring layer is exposed. First, in carrying a passive chip or chip jumpering for forming a bypass capacitor, a filter, etc. in this crevice etc., it is made to stand straight so that only the electrode of one side of these chips may be electrically connected to a wiring substrate, and mounts, and to the height which an upper electrode exposes including the electrode of the chip bottom from a crevice base, the restoration and the cure of the non-conductive closure resin are carried out, and it stiffens it. It enabled it to take electrical installation by contacting a top electrode in a conductive closure resin layer directly by carrying out the restoration and the cure of the conductive closure resin, and furthermore, carrying out the laminating of the electrode of a chip top to wrap height, on non-conductive closure resin.

[0019] moreover, in carrying a semiconductor chip in a crevice The component forming face of a semiconductor chip is carried by the so-called face down placed upside down. To the height which the amount of semiconductor chip flesh-side surface part exposes from this crevice base, carry out the restoration and the cure of the non-conductive closure resin, and it is stiffened. It enables it to have taken electrical installation in the form where the amount of [which the semiconductor chip furthermore exposed on non-conductive closure resin] flesh-side surface part contacts [the amount of flesh-side surface part] conductive closure resin in a conductive closure resin layer directly restoration and by carrying out a cure to wrap height.

[0020] Moreover, when connecting with the stabilization potential to which the conductive closure resin layer itself is supplied from the outside in any [which was mentioned above] case So that electrical installation can be taken to the conductive closure resin with which connects with the circuit pattern corresponding to the stabilization potential in a wiring substrate through chip jumpering, or the crevice of a wiring substrate is filled up beforehand Form the inner conductor layer near a periphery section top face as a whole surface solid pattern, and a shielding layer is formed united with the conductor layer which surrounded and arranged a substrate side face and the base periphery section. It is made to be supplied also at the rear face of a semiconductor chip through conductive closure resin in the stabilization potential supplied to this shielding layer through an external electrode.

[0021] Therefore, conductive closure resin can achieve the duty of shielding.

[0022]

[Example] Next, it explains, referring to a drawing about this invention.

[0023] drawing 1 (a) -- the sectional view of the 1st example of this invention -- it is -- drawing 1 (b) -- it is the top view. Reference of drawing 1 (a) and drawing 1 (b) carries out opening of the crevice 11 to parts other than the periphery section of the top face of multilayer-interconnection substrate 10a which consists of a glass epoxy resin, for example. The magnitude and the depth of this opening are beforehand decided with the magnitude and quantity of the components carried. In order to connect between the component parts carried in the base of a crevice 11 by this opening, the circuit pattern 12 arranged beforehand is exposed. This circuit pattern 12 is suitably connected to the circuit pattern 14 arranged in the rear-face side by the through hole 13 if needed.

[0024] Furthermore, the circuit pattern 14 by the side of a rear face uses a circuit pattern 14 for the end-face electrode 15 indirectly arranged in the substrate periphery section through direct or the carried component part,

and predetermined connection is made. the conductor which this end-face electrode 15 was the so-called external terminal of a package, and set spacing mutually and was put in order -- it consists of a group and has the potential from which plurality differs.

[0025] A semiconductor chip 16 and the passive chips 17a-17f containing chip jumpering are carried in the crevice 11 of the wiring substrate 10 mentioned above. As for this semiconductor chip 16, bump connection of each electrode is made by the face down at the circuit pattern 12, respectively.

[0026] On the other hand, in this example, although two electrodes with which the chip itself has in the case of the conventional example were connected to the circuit pattern 12 by the side of a crevice base, respectively, where only the electrode of one side is connected to a circuit pattern 12, respectively, the passive chips 17a-17f stand straight, and are carried.

[0027] As for the crevice 11, it fills up the rear face of a semiconductor chip 16, and the electrode of the other side of the passive chips 17a-17f with non-conductive closure resin 18 (the slash-like mesh in drawing shows) from the base to its height which carries out **** exposure. On this non-conductive closure resin 18, it fills up with conductive closure resin 19 (a drawing middle point-like mesh shows) to the same height as a substrate periphery section top face, and the resin seal is performed.

[0028] Electrical installation is made by the electrode with which the power-source potential of the end-face electrodes 15 or the stabilization potential of touch-down potential is supplied by chip jumpering 17b from the outside through the predetermined pattern of a circuit pattern 12, a through hole 13, and the circuit patterns 14 (un-illustrating) if conductive closure resin 19 sets for example, chip jumpering to passive chip 17b.

[0029] According to the structure shown in this example, since conductive closure resin 19 connects the rear face of a semiconductor chip 16, and the other side electrode of the passive chips 17a-17b to stabilization potential, a shielding effect can be obtained.

[0030] When drawing 2 (b) which showed drawing 2 R> 2 (a) which showed the 2nd example of this invention with the sectional view, and its top view is referred to, it is an example at the time of constituting the package which has side-face shielding structure. the conductor which the end-face electrode 15 was the so-called external terminal of a package, and set spacing mutually and was put in order in one example of ** -- although it had the potential from which a group is accomplished and plurality differs, in the 2nd example, these serve as a single solid pattern which crossed all over the substrate periphery which has stabilization potentials, such as touch-down potential or power-source potential, and was arranged.

[0031] Namely, while conductive closure resin 19 contacts inner conductor layer 20a of wiring substrate 10b on a crevice inside wall surface, the difference with the 1st example Inner conductor layer 20a is the side-face shielding structure (with a sectional view, it becomes the 20a - abbreviation "character of KO" mold expressed with 20b-20c) extended to side-face 20b and base periphery section 20c of wiring substrate 10b, and it is arranged so that the whole periphery section surface of wiring substrate 10b may be surrounded from a side face. The external electrode 21 is formed in the base periphery section 20c. Further and the circuit pattern 14 by the side of a rear face It is connecting with the external electrode 23 which a circuit pattern's 12 has inside base periphery section 20c of wiring substrate 10b through a through hole 13 indirectly through direct or the carried component part, respectively, and was prepared in the external electrode field 22. Since the other component is the same as that of the 1st example, explanation of a configuration here is omitted.

[0032] According to the configuration of the 2nd example mentioned above, stabilization potential is supplied to the extended inner conductor layers 20a-20c from the external electrode 21, and a shielding effect can be obtained by these extended inner conductor layers 20a-20c.

[0033] In addition, if drawing 3 (a) which prepared the two or more layers electric conduction closure resin layer, and showed the sectional view of a case as a modification of the example mentioned above is referred to, on electric tree fat closure layer 18b, the laminating of electric conduction closure resin layer 19a, non-conducting current resin seal layer 18a, and the electric conduction closure resin layer 19a is carried out one by one, and they are formed. Since the electrode of the other side of the passive chips 17a and 17b is connected to electric conduction closure resin layer 19a and the semi-conductor chip 16 and passive chips [17c and 17d] rear face and an other side electrode are connected to electric conduction closure resin layer 19b, either of different stabilization potentials for every loading components can be divided and supplied.

[0034] Moreover, if drawing 3 (b) which showed the sectional view at the time of preparing two or more crevices is referred to, passive chip 17a and a semiconductor chip 16 are carried in crevice 11a, the passive chips 17b-17d are carried in crevice 11b, and the function which became independent for every crevice, respectively can be given.

[0035] The manufacture approach of ********** explained in the 1st and 2nd examples mentioned above Drawing 4 which is the production process sectional view and showed the bump connection process of a semiconductor chip (a), If drawing 4 (d) which showed the 4th process filled up with drawing 4 R> 4 (b) which the

2nd which pastes up a passive chip ******(ed), drawing 4 (c) which showed the 3rd process which fills up a crevice with non-conductive closure resin, and conductive closure resin is referred to First, it is the wiring substrate with which the crevice was formed in the multilayer-interconnection substrates 10a or 10b formed in the glass epoxy resin substrate by well-known etching processing. At least one semiconductor chip 16 is carried in this crevice by face down by a well-known solder bump's etc. approach (drawing 4 (a)).

[0036] Next, after mounting only the electrode of each one side (below) with electroconductive glue etc., a cure is carried out and it is made to harden, where the passive chips 17a-17f containing the thing for noise filters are uprighted (drawing 4 (b)).

[0037] After an appropriate time, it fills up with predetermined Mr. Fukashi using the high insulating non-conductive closure resin 18 of an epoxy system. At this time, it is filled up with all of all of a part for cover hiding and the flesh-side surface part of a semiconductor chip 16 and a passive chips [17a-17f] top electrode to the height to expose, and before or after 150-degree 30 minutes, the cure of the part which connects with the circuit pattern 12 which touches the bottom electrode of a semiconductor chip 16 and passive chips [17a-17f] each electrically at least is carried out, and they stiffen it (drawing 4 R> 4 (c)).

[0038] Furthermore, after an appropriate time, to wrap height, it is filled up with conductive closure resin 19 with the high electric conductivity of Cu paste etc., and before or after 150-degree 30 minutes, the cure of the top face of non-conductive closure resin 18, and all passive chips [which are exposed from this non-conductive closure resin / 17a-17f] electrodes and the rear face of a semiconductor chip 16 is carried out, and they are stiffened (drawing 4 (d)).

[0039] In addition, after the 4th process, although not shown in drawing, printing formation of the protective layers, such as a resist, may be carried out in the upper part if needed.

[0040] In the manufacture approach of the 2nd example, wiring substrate 10b in the 1st process prepares inner conductor layer 20a in ** which is united with the side-face shielding structures 20b and 20c beforehand as a single solid pattern which crosses all over a substrate periphery and is arranged. In case it closes by conductive closure resin 19, the range of the thickness of the layer of conductive closure resin 19 is taken into consideration, and the location of the height direction of this conductor layer is decided so that the part exposed to the crevice inside wall surface of inner conductor layer 20a may contact the end face of conductive closure resin 19.

[0041] Furthermore, the rear-face side of wiring substrate 10b is the same as that of an above-mentioned production process, except that what the projection electrode 23 as an external terminal was arranged in the substrate periphery section 22 inside side-face shielding structure 20c, and was connected to the circuit pattern 12 at the base of a crevice, respectively is used.

[0042] In addition, when it assumes that the electrolyte thickness whose bump height the thickness of the present semiconductor chip 16 is 0.3mm - about 0.4mm, and is about 0.1mm and the passive chips 17a-17f is around 0.2mm, what is necessary will be just to adjust about the height of non-conductive closure resin 18, i.e., thickness, among about 0.25mm - about 0.35mm.

[0043] Height adjustment with a width of about 0.1mm is satisfactory in any way with the present technique. Of course, when applying to either a semiconductor chip 16 or the passive chips 17a-17f, whenever [allowances / of the width mentioned above since what is necessary was to have taken only one of these into consideration] will spread further.

[0044] As explained above, according to the hybrid integrated circuit equipment and its manufacture approach of this invention As mentioned above, for example, the bypass capacitor and each noise filter between power-source potential and touch-down potential Although it must arrange in the location possible nearest to the semiconductor chip which is a noise generation source, with the hybrid integrated circuit equipment of this invention While the passive chip of the component is uprighted and can be carried, since it is [the everywhere in a crevice] connectable with stabilization potential, the electrode of one side becomes very easy [the pattern layout of a wiring substrate]. Furthermore, since loading area becomes 1/2 or less [original] by making it stand straight, it can arrange easily also near [where a pattern arrangement consistency is high] the semiconductor chip, therefore more effective noise rejection becomes possible.

[0045] moreover, in loading of a semiconductor chip, since a means to connect a part for a flesh-side surface part to stabilization potential easily can be offered, the applicability of flip chip loading is markedly alike, and can extend. As mentioned above, since a wire tends to serve as an antenna, loading area will moreover require twice [about] and the part bypass capacitor and the passive chip for filters will also keep away from a semiconductor chip, the connection by the bonding wire has clearly advantageous loading by the flip chip also in noise.

[0046] Moreover, in a semiconductor chip and passive chip mixture, it is effectiveness with the very effective point that connection with stabilization potential required for especially each can be made by processing of a package, without dividing a process.

[0047] In many cases, by adhesion of a substrate conductor layer, a printing conductor layer, or a shielding metal plate, stable connection cannot be desired from the inequality of the height of loading components, but like the hybrid integrated circuit equipment of this invention, according to restoration of conductive closure resin, the variation in the height of loading components is absorbed entirely, and it becomes possible to obtain stable connection.
[0048] Furthermore, it is also easy to take the electrical installation of conductive closure resin and a substrate inner conductor layer, and if this is used, the good noise shielding structure over the package above connection with the stabilization potential of the external circuit of conductive closure resin itself was completed, therefore they were united with is also realizable for coincidence, as shown in the 2nd example.
[0049] further -- again -- the 2nd example -- like -- the side face of a package -- plating processing etc. -- shielding -- a rear-face solid pattern -- connecting -- a side face -- a conductor -- the solder seal between the MASA boards carrying the lower part and this hybrid integrated circuit equipment etc. is used together, and 20dB - 30dB noise reduction can be performed.
[0050] Moreover, as a secondary effect, according to the structure of this invention, since it is directly in contact with conductive closure resin with large thermal conductivity and the thickness also becomes comparatively thick with hundreds of micro, a semiconductor chip rear face functions also as good heat dissipation structure. especially the case where the shielding structure mentioned above is taken -- the conductor of shielding -- since heat leakage by the side of a wiring substrate is planned through a part, it is more effective.
[0051] The shift of many properties of IC device by heat usually worsens the noise margin to malfunction. Therefore, even if it sees heat dissipation structure from a noise-viewpoint, it is an important element.
[0052]
[Effect of the Invention] As explained above, the hybrid integrated circuit equipment and its manufacture approach of this invention It is the structure which establishes a crevice in a wiring substrate, and carries and carries out the resin seal of a semiconductor chip, a passive chip, or its both to this crevice. By arranging the rear face of a semiconductor chip, and the electrode of one side of a passive chip with the sense above a crevice by carrying a semiconductor chip by face down to a crevice base, uprighting a passive chip and carrying While forming the condition of having detached perpendicularly to the electrode of the other side linked to a base It has the multilayer structure containing the non-conductive closure resin layer to which the resin for the crevice closures touches a crevice base, and the conductive closure resin layer of the upper layer. To the height which the electrode of one side of a part for a semiconductor chip flesh-side surface part and a passive section chip exposes from a crevice base, carry out the restoration and the cure of the non-conductive closure resin, and it is stiffened. Conductive closure resin on non-conductive closure resin to wrap height for a part for the flesh-side surface part furthermore exposed, and the electrode of one side restoration and by carrying out a cure Since it enabled it to take electrical installation where a part for a flesh-side surface part and the electrode of one side are directly contacted in a conductive closure resin layer, respectively By connecting a conductive closure resin layer to stabilization potential through an external terminal, a conductive closure resin layer can achieve a very effective shielding effect to a noise.
[0053] Moreover, since it can also consider as the shielding structure it was made united [structure] with the conductor layer which surrounded a substrate side face and the base periphery section, and formed the inner conductor layer of the substrate periphery section which was made to carry out end-face contact with a conductive resin layer, the same shielding effect is obtained.
[0054] Furthermore, since both the high layout of the degree of freedom of the filter element by easy-izing of flip chip loading application and the passive chip good shielding structure and heat dissipation structure are realizable for coincidence, the cure against a noise can carry out very easily and effectively, and makes it possible to fully pull out the engine performance of device original.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (a) It is the sectional view showing the hybrid integrated circuit equipment of the 1st example of this invention.
(b) It is the top view of the 1st example.
[Drawing 2] (a) It is the sectional view showing the hybrid integrated circuit equipment of the 2nd example of this invention.
(b) It is the top view of the 2nd example.
[Drawing 3] (a) Prepare a two or more layers electric conduction closure resin layer, and it is the sectional view of a case.
(b) It is a sectional view at the time of preparing two or more crevices.
[Drawing 4] (a) It is the sectional view having shown the bump connection process of a semiconductor chip.
(b) It is the sectional view which the 2nd which pastes up a passive chip ******(ed).
(c) It is the sectional view having shown the 3rd process which fills up a crevice with non-conductive closure resin.
(d) It is the sectional view having shown the 4th process filled up with conductive closure resin.
[Drawing 5] It is the sectional view showing an example of conventional hybrid integrated circuit equipment.
[Drawing 6] It is the sectional view showing other examples of conventional hybrid integrated circuit equipment.
[Description of Notations]
10a, 30, 43 Wiring substrate
10b The wiring substrate which has side-face shielding structure
11, 11a, 11b 31 Crevice
12 34 Circuit pattern by the side of a base
13 38 Through hole
14 37 Circuit pattern by the side of a rear face
15 End-Face Electrode
16 32 Semiconductor chip
17a-17f, and 33a- 33c and 42 Passive chip
18, 18a, 18b, 36 Non-conducting current closure resin
19, 19a, 19b Conductive closure resin
20a Inner conductor layer (conductor solid pattern)
20b Side-face shielding of the wiring substrate 10
20c Base periphery section shielding
21 22 Projection electrode (external electrode)
23 External Electrode Field
35 44 Wire
39 Shielding Plate
40a, 40b Loading electrode
41a The top electrode of a passive chip
41b The bottom electrode of a passive chip

[Translation done.]

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